MOEM

Modern Electronic Materials 4(4): 143–150
DOI 10.3897/j.moem.4.4.39503

Research Article

Contact and contactless porous silicon parameter measurement techniques

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Received 16 October 2018 ♦ **Accepted** 22 November 2018 ♦ **Published** 1 December 2018

Citation: Latukhina NV, Kobeleva SP, Rogozhina GA, Shishkin IA, Schemerov IV (2018) Contact and contactless porous silicon parameter measurement techniques. Modern Electronic Materials 4(4): 143–150. https://doi.org/10.3897/j.moem.4.4.39503

Abstract

In this work we have used contact and contactless techniques to measure the electrical resistivity of single crystal silicon wafers with porous layers of variable thickness synthesized on the surface. The porous layers have been synthesized on the surfaces of single crystal wafers with well pronounced microroughness pattern, either textured or grinded. We have used the classic four-probe method with a linear probe arrangement as the contact measurement technique, and the resonance microwave method based on microwave absorption by free carriers as the contactless measurement technique. Electrical resistivity distribution over the specimen surface has been mapped based on the measurement results. We have demonstrated a general agreement between the electrical resistivity distribution patterns as measured using the contact and contactless measurement techniques. To analyze the electrical resistivity scatter over the specimen surface area we have simulated the field distribution in the electrolyte during porous layer formation in a non-planar anode cell. The regularities of the electrical resistivity spatial distribution in different types of specimens are accounted for by specific porosity formation mechanisms which in turn are controlled by the initial microroughness pattern and the field distribution pattern in the electrolyte for each specific case.

Keywords

porous silicon, electrical resistivity, contactless method, four-probe method, electrochemical etching

1. Introduction

Contactless parameter measurement techniques are of special interest for nanomaterials which include porous silicon because contact measurement of their parameters may cause irreversible damage to their nanostructure. An urgent problem is the treatise of nanomaterial parameter contactless measurement results and their comparison with conventional contact technique data.

Electrical resistivity of porous silicon may very over an extremely wide range [1–3]. It depends on the porous layer technology used and on the initial material properties. The electrical resistivity distribution pattern over the porous layer surface is directly related to the electric field propagation in the electrolyte and at the silicon/electrolyte boundary. Porosity formation in silicon structures during chemical and electrochemical etching has been simulated using a large number of models providing, to different extents, sufficient explanation of the physical regularities of this phenomenon [1–6]. There are several physical models [4–9] interpreting some porosity formation aspects from the standpoints of instability of the planar silicon/

electrolyte boundary against small periodical disturbance under electrochemical etching conditions and anode current localization at the concave bottom surfaces of the growing pores. In turn, chemical models concentrate on the explanation of the effective silicon valence and hydrogen release mechanisms accompanying the transfer of silicon atoms to the electrolyte from the surface layer [10, 11]. There are studies [9, 12] of the contribution of valence band holes as a necessary condition for silicon dissolution in HF base electrolytes and factors determining the transition from porosity formation to continuous etching of silicon specimens; an adapted model was suggested (for the A^3B^5 compounds) [10, 13] describing self-organizing cooperative nucleophilic substitution reactions between chemisorbed anions and coordination-saturated atoms of the surface crystal lattice layer initiated by the barrier jump field at the electrolyte/semiconductor phase boundary. Along with porosity formation physical models there are numerous studies dealing with mathematical and computer simulation of the process [7, 8, 11–16]. However the problem of the porosity spatial distribution over specimen surface and the effect of the field on the distribution are studied but little though this aspect is quite important for the device applications of porous silicon structures. Most porosity formation models suggested earlier do not take into account the effect of microroughness at the silicon wafer surface, the anode/electrolyte boundary being usually considered planar. The importance of this work is demonstration of a direct relationship between the field distribution in the electrolyte volume and at the electrolyte/semiconductor boundary and the initial surface morphology with the final porous layer parameters.

2. Materials and experimental

The porous silicon layer was synthesized on the wafer surface by electrochemical etching in hydrofluoric acid alcohol/water solutions in vertical electrolytic cells. We used *p*-type single crystal silicon wafers with grinded or textured (with regular rectangular pyramids) surfaces. Porosity formation on this type of surfaces occurs predominantly in microroughness cavities [1, 17]. The surfaces of the grinded wafers were oriented along the (111) crystallographic plane and those of the textured wafers, along the (100) planes. The specimens were 2.5 cm sided quadrates.

The electrical resistivity of the specimens was measured with two techniques, i.e., the classic four-probe method with a linear probe arrangement and, as the contactless measurement technique, the resonance microwave method based on microwave absorption by free carriers for it allows measurements to be carried out without introducing contamination or damaging the surface structure of the specimens. The four-probe method was used for calibrating the contactless method.

The operation principle of the BKI-UES contactless measurement instrument is as follows. A *p–n–p* bipolar transistor (e.g. KT-647) base generator produces a 5 GHz standing wave in the resonator in the form of a rectangular waveguide. One of the waveguide walls has an opening from which part of the microwave radiation is output through an antenna installed in front of the opening. If the opening is blocked by a semiconductor part of the microwave radiation is absorbed by the free carriers. Recording the resultant change in the microwave radiation power inside the waveguide one can estimate the carrier concentration. The output signal is detected with a D602 microwave detecting diode and amplified with a KR544UD2 broadband amplifier. The amplified signal is fed to a Fractal MSKh52-3 microcontroller built on the basis of a PIC18 module the microcontroller of which digitizes the signal and provides PC communication [18].

The contactless microwave method is a calibrated one, i.e., the output signal expressed in relative units can be converted to electrical resistivity only by comparing with results for similarly shaped specimens having known electrical resistivity. For this experiment we measured the specimens simultaneously with the contactless and the four-probe techniques in order to immediately convert the output signal to electrical resistivity units. This eliminated the necessity of using reference specimens.

Four-probe measurements were carried out with a VIK-UES-A instrument at 80 points with a 2 mm steps over the area of a circle inscribed into a square wafer. Series of three measurements for each wafer were taken for average value calculation at each point and plotting a color 3D map of electrical resistivity distribution over the specimen surface which illustrated its inhomogeneity. Contactless measurements were carried out with 5 mm steps at 20 points along the quadrate diagonal.

3.1. Simulation of field distribution in electrolyte volume during electrolytic etching

This work was aimed at simulating the field distribution in the electrolyte at the silicon/electrolyte boundary and comparing it with the electrical resistivity distribution maps. We studied the 2D electric fields by analyzing the potential distribution along planes perpendicular to the electrodes. Before an external current source is switched on, an electrode potential exists in the system due to the double electric field at the semiconductor/electrolyte boundary: the polarized molecules of the solution cause ions in the surface semiconductor layer to hydrate and transfer to the solution thus charging it positively, while the excess electrons in the semiconductor produce a negative charge. The negative charge at the electrode prevents cation transfer to the solution while part of the cations in the solution interact with electrons and enter the sites of the crystal lattice they left. A dynamic equilibrium is established when the cation emission and return rates equalize. This results in the generation of a double electric layer similar to a flat capacitance one plate of which is the semiconductor surface and the other is the layer of ions in the electrolyte solution. The electrode potential as

a function of the cation concentration in the solution and the temperature is described by the Nernst equation:

$$\varphi = \varphi^0 + \frac{RT}{nF}\ln\frac{a(ox)}{a(red)}, \quad (1)$$

where φ^0 is the standard electrode potential, n is the number of electrons involved in the reaction, F is the Faraday constant, R is the universal gas constant and a(ax), a(red) are the activities of the oxidizing and reducing forms, respectively.

Once an external voltage source is connected to the system, current starts passing through the electrolytic bath resulting in a shift of the potentials from the equilibrium values, i.e., to electrode polarization. The chemical polarization of the electrodes produces a voltaic cell with the electromotive force direction opposite to that of the external electromotive force. Therefore the voltage of electrolysis is generally the sum of the polarization electromotive force, the anodic and cathodic overvoltages and the ohmic potential drop at the electrolyte. For the case in question the electrolysis reaction at the electrode/electrolyte boundary is so intense that the electrode kinetics can be neglected and the barrier potential difference deviates from its equilibrium value but slightly. In other words there is no activation overvoltage and hence the current distribution only depends on the anode and cathode shapes. For the textured surface specimens the anode was a regular array of similar regular triangles and for the grinded surface specimens, an irregular array of differently sized triangles.

The field was computer simulated using the COMSOL Multiphysics software package (for electrochemical cell simulation). The boundary conditions were as follows: the electrolyte was considered electrically neutral uncompressible liquid with negligible composition variation and no turbulence, P = 1 atm, T = 293 K, ρ and μ are constant.

The main equations used for the computer model were as follows: diffusion current as a function of ion concentration and electrical field magnitude in the electrolyte was described using the Nernst–Plank equation:

$$J_m = -D\nabla c - U_m ZFc\nabla\varphi, \quad (2)$$

where J_m is the ion molar flow density, mol×s^{-1}cm^{-2}; D is the diffusion coefficient, cm^{2}s^{-1}; c is the ion concentration, mol×cm^{-3}; U_m is the molar ion mobility ($U_m = D/RT$), cm^{-2}mol×s^{-1}Cl^{-1}V^{-1}; Z is the charge number, F is the Faraday constant, Cl mol^{-1} ($F = eN_a$); field magnitude expressed via potential gradient.

The current density in the electrolyte is

$$j_l = -\delta_l\nabla\varphi_l. \quad (3)$$

The current density at the electrode is

$$j_s = -\delta_s\nabla\varphi_s, \quad (4)$$

where δ_l, δ_s is the conductivity of the material preset in the model.

The calculation results were presented in the form of current density vector field map in the plane perpendicular to the wafer surface. Since the electric field and the current density are in simple relationships such as Eqs. (3)–(4), the current density vector field maps will be identical to the electrolyte field distribution maps.

3. Results and discussion

The four-probe electrical resistivity measurement results are summarized in Table 1. Fig. 1*a–c* show experimental electrical resistivity distribution maps over specimen surface for specimens with porous layers formed on textured surfaces subjected to etching for different times. The measurements showed that the average electrical resistivity of the initial wafers with textured surface is 1.96 ± 0.12 Ohm×cm, the difference between the highest and the lowest electrical resistivity being 1 Ohm×cm, i.e., more than 50% of the average value. The differently colored regions in the Figure (with different electrical resistivities) have almost equal areas and are distributed over the wafer surface almost homogeneously. Porous layer formation increases the average electrical resistivity and somewhat increases the homogeneity of its distribution over the specimen surface. After porous layer formation for 5 min the average electrical resistivity increases to 3.20 ± 0.11 Ohm×cm, the difference between the highest and the lowest electrical resistivity decreases to 22% for the maximum value and the area of homogeneous regions increases considerably (Fig. 1*b*). For 10 min etching the homogeneity increases further although the average electrical resistivity decreases to 2.10 ± 0.34 Ohm×cm (Fig. 1*a*). For this etching mode the pyramids

Table 1. Specimen parameters as measured by four-probe technique.

Specimen #	Surface type	ρ_{max}, Ohm·cm	ρ_{min}, Ohm·cm	ρ_{av}, Ohm·cm	$(\rho_{max} - \rho_{min})/\rho_{av}$	RMS Δρ, Ohm·cm	$\Delta\rho/\rho_{av}$, %
T0	Initial textured	2.3	1.3	2	0.5	0.13	7
T5	Textured with porous layer, 5 min etching	3.5	2.8	3.2	0.22	0.12	4
T10	Textured with porous layer, 10 min etching	2.4	1.95	2.1	0.21	0.09	5
Sh0	Initial grinded	2.1	1.3	1.6	0.57	0.12	8
Sh1	Grinded with porous layer, 5 min etching	2.5	1.8	2.2	0.32	0.13	6
Sh2	Grinded with porous layer, 10 min etching	2.23	1. 01	1.9	0.63	0.15	8
Sh3	Grinded with porous layer, 15 min etching	4.00	1.8	2.3	0.96	0.4	17
Sh3 (fragm.)	Grinded with porous layer, 15 min etching	4.00	3.4	2.3	0.26	–	–

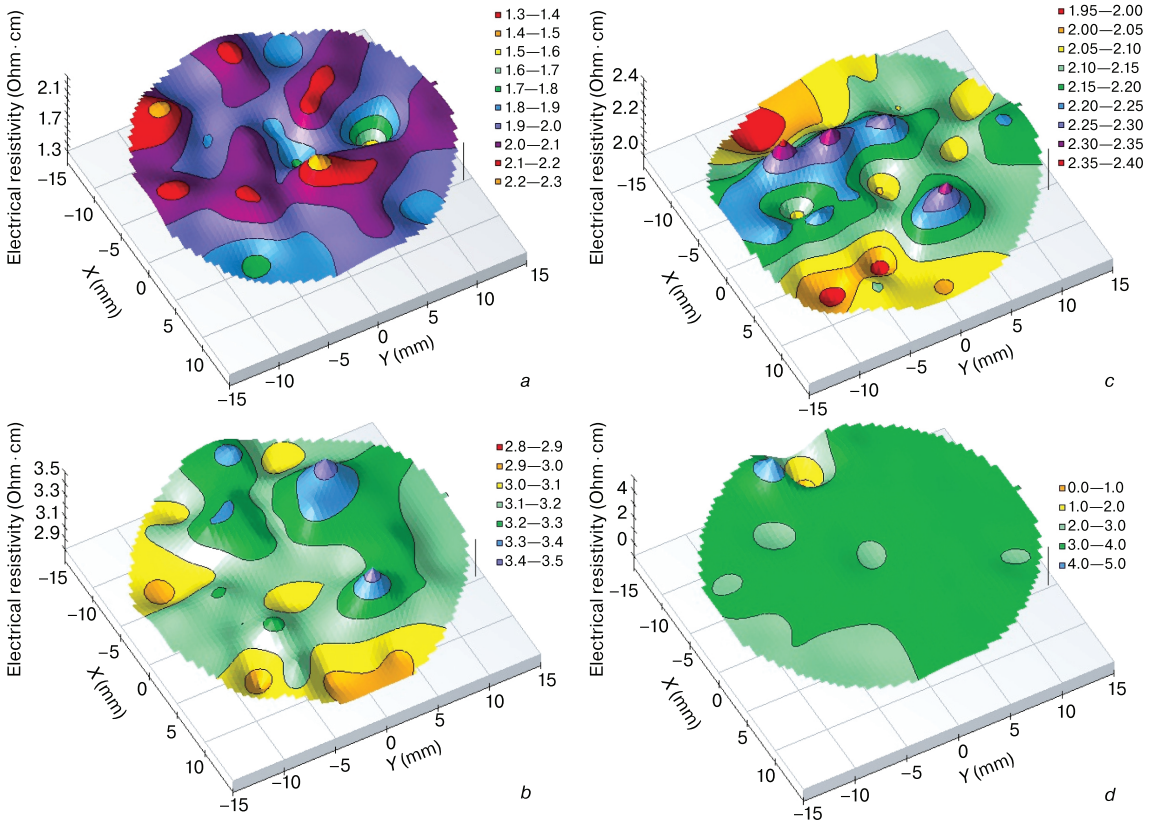

Figure 1. Four-probe technique electrical resistivity distribution over textured specimen surface: (*a*) initial textured surface, ρ_{av} = 2±0.13 Ohm×cm; (*b*) surface with porous layer formed in 5 min, ρ_{av} = 3.2±0.11 Ohm×cm; (*c*) same with 10 min etched porous silicon layer, ρ_{av} = 2.13±0.09 Ohm×cm; (*d*) same with 15 min etched porous silicon layer, ρ_{av} = 3.1±0.5 Ohm×cm.

acquire equal height since almost all small pyramids are etched off to form the porous layer surrounding larger pyramids [19]. Longer etching for 15 min causes regions with equal electrical resistivity to split again into smaller ones, with the average electrical resistivity still decreasing, but large pyramids start dissolving instead of pore depth growth and hence the roughness is smoothed. All the etched specimens exhibit asymmetry in the resistivity distribution: the electrical resistivity is higher at one wafer side. The same holds for the electrical resistivity distribution along the quadrate diagonal for contactless measurement results (Fig. 2*a*, *b*), i.e., there is a correlation between the contact and contactless measurement data. The asymmetry is caused by the effect of gravity on the ion transport in the electrolyte for vertical wafer arrangement in the electrolytic cell. Furthermore both the contact and contactless techniques suggest that the resistivity at wafer sides is lower than in the center which also agrees with the simulated field distribution in the electrolyte (Fig. 3). The current density vector field map (Fig. 3) shows that the current density vector component perpendicular to the wafer plane is the largest in the wafer center whereas the tangential component increases as one approaches the sides. The potential difference between the wafer center and the sides is more than 10 V. As a result slot-shaped pores form more intensely in the center and the porous

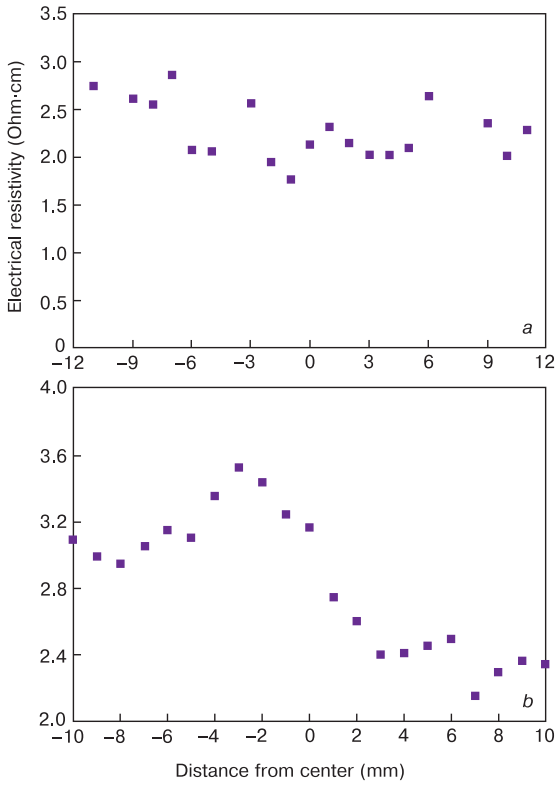

Figure 2. Contactless technique electrical resistivity distribution along quadrate diagonal for textured specimens with (*a*) 10 min and (*b*) 15 min etched porous silicon layer.

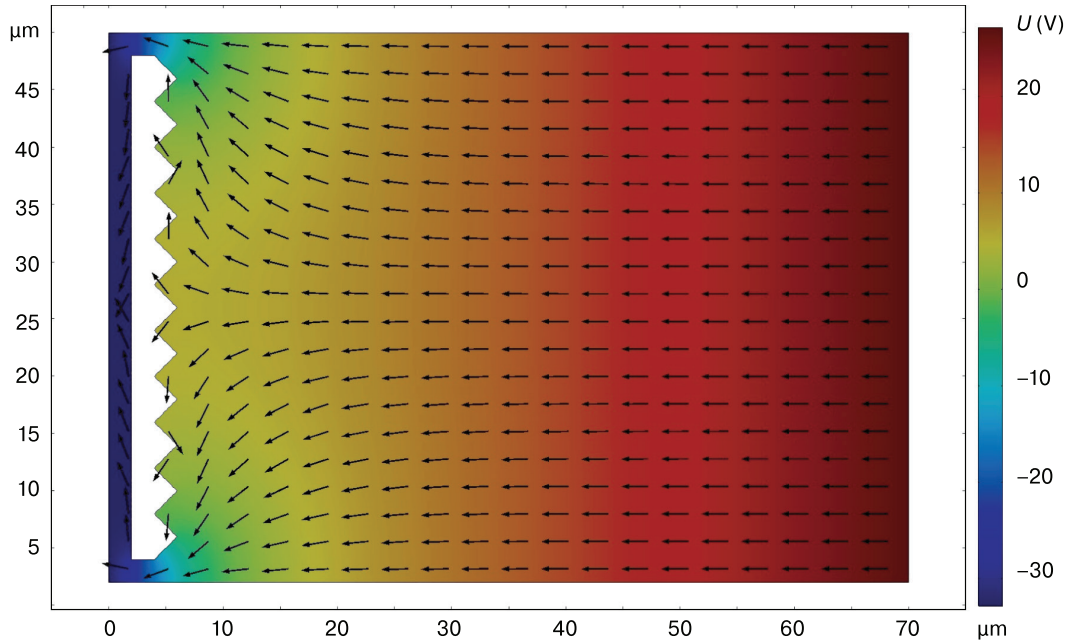

Figure 3. (arrows) field magnitude and (color) potential distribution in electrolyte for textured specimen etching. Left-hand digital *y*-axis and *x*-axis define electrolyte section area by plane perpendicular to wafer surface; right-hand digital *y*-axis combined with color axis defines potential values.

Table 2. Specimen parameters as measured by contactless technique.

Specimen #	Surface type	ρ_{max}, Ohm·cm	ρ_{min}, Ohm·cm	ρ_{av}, Ohm·cm	$(\rho_{max} - \rho_{min})/\rho_{av.}$	RMS Δρ, Ohm·cm	$\Delta\rho/\rho_{av.}$, $\%_{av}$
2 T	Textured with porous layer, 10 min etching	3.5	2.2	2.8	0.48	0.5	15
9T	Textured with porous layer, 15 min etching	2.9	1.7	2.2	0.5	0.3	14
Sh1	Grinded with porous layer, 10 min etching	4.6	1.5	1.8	1.7	0.4	19
Sh1 (w/o spike)	Grinded with porous layer, 10 min etching	1.9	1.5	1.7	0.25	0.14	8

layer is thicker there than at the edges, hence the electrical resistivity is higher in the center.

Analysis of the results for specimens with grinded surfaces (Fig. 4*a–d*; Fig. 5*b*) suggests other conclusions. According to contact four-probe technique the parameter describing the difference between the highest and the lowest electrical resistivity as well as the RMS deviation for the specimens with initially textured and initially grinded surfaces are nearly the same, e.g. $(\rho_{max} - \rho_{min})/\rho_{av} = 0.57$ for textured surface, $(\rho_{max} - \rho_{min})/\rho_{av} = 0.5$ for grinded surface, and RMS deviation is 8% for grinded surface and 7% for textured surface. However the distribution of regions with different electrical resistivity over grinded specimen surface is inhomogeneous unlike the homogeneous distribution for textured specimens, and this "edge effect" cannot be attributed to gravity as for etched specimens.

The homogeneity degrees of the grinded specimens with porous layers and specimens with the porous layers on textured surfaces differ for similar etching time. After 5 min etching both specimen types exhibit an increase in the homogeneity with an increase in the average resistivity. For 10 min etching both these parameters increase in the specimens with etched surfaces unlike those with textured surfaces. For this etching mode the etched surfaces have no more small inhomogeneities and pores form intensely in microroughness cavities. For the specimens with porous silicon layers on grinded surfaces after 15 min etching the homogeneity increases, the difference between the highest and the lowest electrical resistivity being the smallest (except for a small spike region where the electrical resistivity differs largely from that in other regions) which is not the case for the specimens with textured surfaces. This behavior can be accounted for by field distribution regularities in the electrolyte for grinded anode surface (Fig. 5). Unlike textured surfaces the potential difference between the center and the edges of grinded wafers is far lower than 10 V and the tangential current density component is comparable with the surface-average one. Therefore porous layer formation is accompanied by microroughness smoothing.

Comparison of the electrical resistivity distributions for contact four-probe method and along the diagonal of the specimens according to the contactless technique (Fig. 6) for the grinded specimen etched for 10 min shows

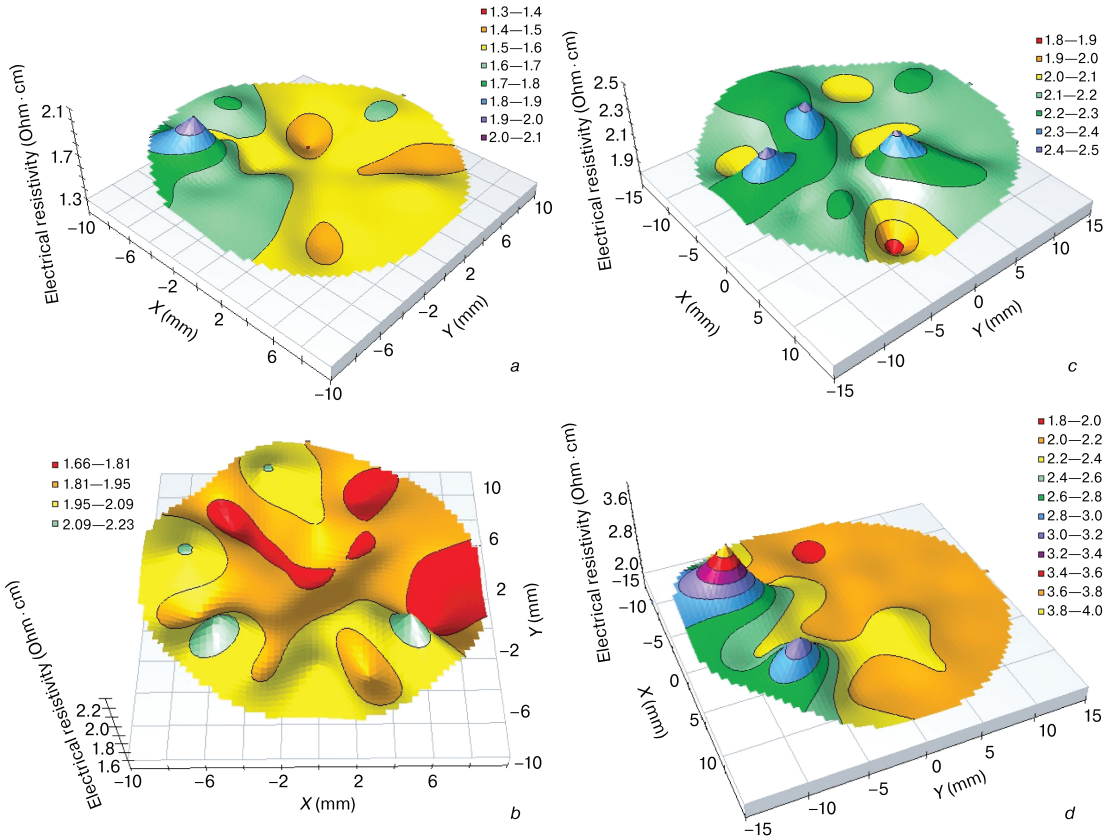

Figure 4. Four-probe technique electrical resistivity distribution over grinded specimen surface: (*a*) initial textured surface, ρ_{av} = 1.57±0.11 Ohm×cm; (*b*) surface with porous layer formed in 5 min, ρ_{av} = 1.91±0.14 Ohm×cm; (*c*) same with 10 min etched porous silicon layer, ρ_{av} = 2.18±0.13 Ohm×cm; (*d*) same with 15 min etched porous silicon layer, ρ_{av} = 2.3±0.4 Ohm×cm.

Table 3. Data comparison between contact and contactless techniques.

Specimen #	Contact / Contactless	Surface type	ρ_{max}, Ohm·cm	ρ_{min}, Ohm·cm	ρ_{av}, Ohm·cm	$(\rho_{max} - \rho_{min})/\rho_{av.}$	RMS Δρ, Ohm·cm	Δρ/$\rho_{av.}$, %
2T	CL	Textured with porous layer, 10 min etching	3.5	2.1	2.8	0.5	0.7	25
T10	C	Textured with porous layer, 10 min etching	2.4	1.95	2.1	0.21		40
9T	CL	Textured with porous layer, 15 min etching	2.9	1.7	2.2	0.5	1	50
T7	C	Textured with porous layer, 15 min etching	4	2	3	0.67		30
Sh2	C	Grinded with porous layer, 10 min etching	2.2	1.1	1.9	0.63	0.24	13
Sh1 (w/o spike)	CL	Grinded with porous layer, 10 min etching	1.9	1.5	1.7	0.13		15

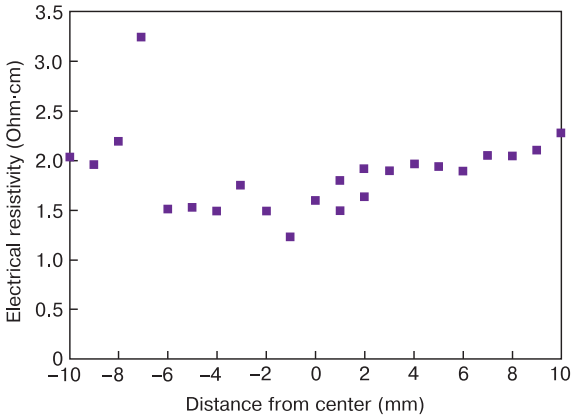

Figure 5. Contactless technique electrical resistivity distribution along quadrate diagonal for grinded specimens with 10 min etched porous silicon layer.

a good agreement between the values by magnitude, scatter and spatial distribution. The highest electrical resistivity yielded by the contactless technique is 2.2 Ohm·cm and the average one is 1.9 ± 0.14 Ohm·cm whereas for the contact technique these figures are 2 Ohm·cm and 1.7 ± 0.13 Ohm·cm, respectively (Table 3).

4. Conclusion

Analysis of the results leads to the following practically useful conclusions.

1. The electrical resistivity distribution over porous silicon surface depends on the initial surface microroughness and electrolytical etching time;

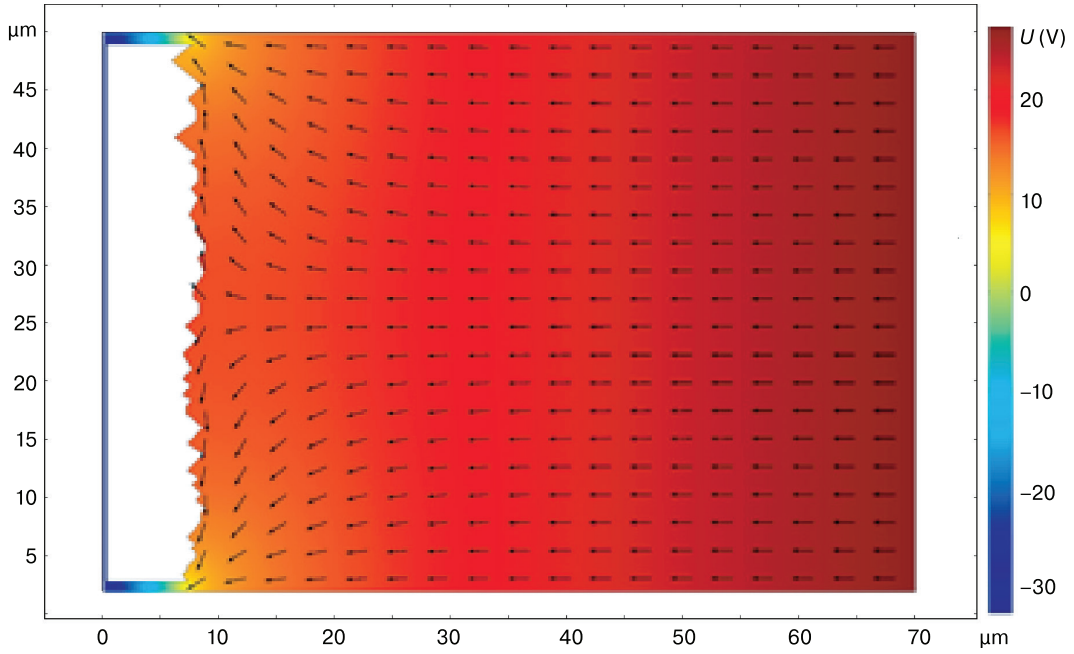

Figure 6. (arrows) current density and (color) potential distribution in electrolyte for grinded specimen etching.

2. Field distribution simulation for electrochemical etching suggests that at the silicon anode/electrolyte boundary it is controlled by the initial surface microroughness;
3. Taking into account the inhomogeneity of the initial materials and the difference in the electrical resistivity measurement techniques one can accept that the electrical resistivity distribution patterns over the wafer surface are roughly the same for contact and contactless measurements and correspond to the electrical field distribution in the electrolyte;
4. The numeric parameters yielded by contact and contactless measurements correlate. The difference between the average electrical resistivities of the same specimen types for contact and contactless measurements is of the same order of magnitude or smaller than the difference between the highest and the lowest electrical resistivity for the specimens.

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